

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

KARSTEN WIECZOREK
MANFRED HORSTMANN
ROLF STEPHAN

Group Art Unit: Unknown

Examiner: Unknown

Serial No.: Unknown

Att'y Docket: 2000.104300/DE0116


Filed: Concurrently Herewith

For: METHOD OF REMOVING FEATURES
USING AN IMPROVED REMOVAL
PROCESS IN THE FABRICATION OF
A SEMICONDUCTOR DEVICE

SUBMISSION OF PRIORITY DOCUMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

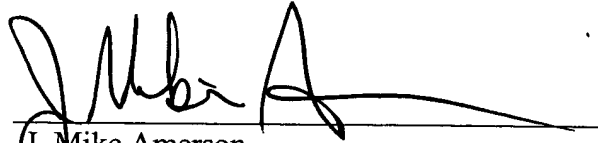
EXPRESS MAIL RECEIPT	
NUMBER:	EV 291395819 US
DATE OF DEPOSIT:	July 22, 2003
I hereby certify that this paper or fee is being deposited with the United States Postal Service "EXPRESS MAIL POST OFFICE TO ADDRESSEE" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
 Signature	

Transmitted for filing herewith is the certified copy of the priority document – German Patent Application No. 102 50 902.6 filed on October 31, 2002.

If any fees under 37 C.F.R. §§ 1.16 to 1.21 are required for any reason relating to the enclosed materials, the Assistant Commissioner is authorized to deduct said fees from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/DE0116.

Please date stamp and return the accompanying postcard to evidence receipt of this document.

Respectfully submitted,



J. Mike Amerson

Reg. No. 35,426

WILLIAMS, MORGAN & AMERSON

10333 Richmond, Suite 1100

Houston, Texas 77042

(713) 934-4055

(713) 934-7011 (facsimile)

ATTORNEY FOR APPLICANTS

Date: July 22, 2003



23720

PATENT TRADEMARK OFFICE

BUNDESREPUBLIK DEUTSCHLAND



Prioritätsbescheinigung über die Einreichung einer Patentanmeldung

Aktenzeichen: 102 50 902.6

Anmeldetag: 31. Oktober 2002

Anmelder/Inhaber: ADVANCED MICRO DEVICES, INC., Sunnyvale,
Calif./US

Bezeichnung: A method of removing features using an improved
removal process in the fabrication of a semiconductor
device

IPC: H 01 L 21/336

Die angehefteten Stücke sind eine richtige und genaue Wiedergabe der ursprünglichen Unterlagen dieser Patentanmeldung.

München, den 24. Februar 2003
Deutsches Patent- und Markenamt
Der Präsident
Im Auftrag

A handwritten signature in black ink, appearing to read 'J. Waasmaier'.

Waasmaier



GKS & S MAXIMILIANSTRASSE 58 D-80538 MÜNCHEN GERMANY

RECHTSANWÄLTE
LAWYERS

MÜNCHEN
DR. HELMUT EICHMANN
GERHARD BARTH
DR. ULRICH BLUMENRÖDER, LL.M.
CHRISTA NIKLAS-FALTER
DR. MAXIMILIAN KINKELDEY, LL.M.
DR. KARSTEN BRANDT
ANJA FRANKE, LL.M.
UTE STEPHANI
DR. BERND ALLEKOTTE, LL.M.
DR. ELVIRA PFRANG, LL.M.
KARIN LOCHNER
BABETT ERTLE

PATENTANWÄLTE
EUROPEAN PATENT ATTORNEYS

MÜNCHEN
DR. HERMANN KINKELDEY
PETER H. JAKOB
WOLFHARD MEISTER
HANS HILGERS
DR. HENNING MEYER-PLATH
ANNELIE EHNOLD
THOMAS SCHUSTER
DR. KLARA GOLDBACH
MARTIN AUFENANGER
GOTTFRIED KLITZSCH
DR. HEIKE VOGELSANG-WENKE
REINHARD KNAUER
DIETMAR KUHLE
DR. FRANZ-JOSEF ZIMMER
BETTINA K. REICHELT
DR. ANTON K. PFAU
DR. UDO WEIGELT
RAINER BERTRAM
JENS KOCH, M.S. (U of PA) M.S.
BERND ROTHAEDEL
DR. DANIELA KINKELDEY
DR. MARIA ROSARIO VEGA LASO
THOMAS W. LAUBENTHAL
DR. ANDREAS KAYSER
DR. JENS HAMMER
DR. THOMAS EICKELKAMP

PATENTANWÄLTE
EUROPEAN PATENT ATTORNEYS

BERLIN
PROF. DR. MANFRED BÖNING
DR. PATRICK ERK, M.S. (MIT)

KÖLN
DR. MARTIN DROPMANN

CHEMNITZ
MANFRED SCHNEIDER

OF COUNSEL
PATENTANWÄLTE

AUGUST GRÜNECKER
DR. GUNTER BEZOLD
DR. WALTER LANGHOFF

DR. WILFRIED STOCKMAIR
(-1996)

IHR ZEICHEN / YOUR REF.

UNSER ZEICHEN / OUR REF.

DATUM / DATE

P 33158-04553/we

31.10.02

Applicant: ADVANCED MICRO DEVICES, INC.

One AMD Place, Mail Stop 68,

Sunnyvale, CA 94088-3453

USA

**A METHOD OF REMOVING FEATURES USING AN IMPROVED
REMOVAL PROCESS IN THE FABRICATION OF A
SEMICONDUCTOR DEVICE**

A METHOD OF REMOVING FEATURES USING AN IMPROVED REMOVAL PROCESS IN THE FABRICATION OF A SEMICONDUCTOR DEVICE

FIELD OF THE PRESENT INVENTION

The present invention relates to the field of fabrication of integrated circuits, and more particularly to a method for improving the etch behavior of semiconductor device features.

DESCRIPTION OF THE PRIOR ART

The fabrication of integrated circuits requires tiny features of precisely controlled shape and size, for example, a gate electrode, to be formed in a layer of material on an appropriate substrate, such as a silicon substrate. With increasing integration density of the integrated circuits, it becomes more and more crucial to reliably and reproducibly create the minimum feature size, also referred to as critical dimension (CD), within a specific layer of material. The tiny features of precisely controlled shape and size are generated by treating the layer of material by means of, for example etching, wherein a mask layer is formed over the layer of material to define the tiny features in the layer of material. In general, a mask layer may consist of a layer of photo resist being patterned by a photo-lithographic process.

During the photo-lithographic process, the photo resist may be spin coated onto the wafer substrate and subsequently selectively exposed to deep ultra violet radiation. Bottom anti-reflective coating (BARC) layers are required to minimize reflections and corresponding stray light exposure during the photolithography process. Without a buried anti-reflective coating layer exposure of the highly sensitive photo resist in undesired regions might be caused by light reflected at underlying layers. Therefore controlling of the critical dimensions, i. e. the size and shape of the tiny features, may be more difficult. Thus, buried anti-reflective coating layers are essential in the fabrication of field effect transistors in Ultra-Large-Scale-Integrated (ULSI) devices. Typically, inorganic materials such as silicon nitride (SiN) are

employed to form the buried anti-reflective coating layer. The buried anti-reflective coating layer may also act as an etch stop layer in the subsequent etch process structuring the photo resist layer, the antireflective coating layer and the layer of material, to form the tiny regions. After the removal of the residual photo resist layer the structured anti-reflective coating layer is removed in a further etch process. A silicon nitride removal process typically employs hot phosphoric acid. The etch selectivity of the antireflective coating layer to the layer of material, however, may be poor, particularly when the buried anti-reflective coating layer is formed of silicon nitride and the gate electrode material is doped polysilicon. Predoped polysilicon, for example, is used in advanced field effect transistors to form the gate electrode to reduce undesired gate depletion. Doped polysilicon shows a higher etch rate compared to undoped polysilicon. The poor etch selectivity leads to an increased surface roughness and makes controlling of the critical dimension of the feature more difficult, which may affect the device performance or even lower the production yield of devices.

To explain in detail the use of buried anti-reflective coating layers, according to a typical prior art process sequence, the process flow for forming a gate electrode of a MOS-field effect transistor is described with reference to Figs. 1a-1d, schematically depicting cross-sectional views of a partially formed field effect transistor.

Fig. 1a schematically depicts a semiconductor structure 1 comprising a silicon substrate 10 with shallow trench isolation (STI) regions 20, a gate insulation layer 30, a polysilicon layer 40 and a buried anti-reflective coating layer 50 formed thereon.

A typical process flow for forming the semiconductor structure 1 includes well known isolation and deposition techniques and thus, a description thereof will be omitted.

Fig. 1b depicts the semiconductor structure 1 after the formation of a gate electrode 41. The semiconductor structure 1 thus comprises the silicon substrate 10, the shallow trench isolation regions 20, a structured gate insulation layer 31, the gate

electrode 41, a structured buried anti-reflective coating layer 51 and a resist feature 61.

Forming the gate electrode 41 may include a photolithography process, wherein the buried anti-reflective coating layer 50 reduces the reflection of light at the underlying interfaces during the exposure of the photo resist. The buried anti-reflective coating layer 50 may further act as an etch stop layer in the subsequent etch process. The etching of the resist layer and of the polysilicon layer 40 is typically performed in an anisotropic plasma etch process.

Fig. 1c depicts the semiconductor structure 1 after removal of the photo resist feature 61. The removal of the photo resist is typically performed by the use of an etch process.

Fig. 1d depicts the semiconductor structure 1 with the completed gate electrode 41. The structured buried anti-reflective coating layer 51 is removed so that the semiconductor structure 1 comprises the silicon substrate 10, the shallow trench isolation regions 20, the gate insulation layer 31 and the gate electrode 41.

The silicon nitride buried anti-reflective coating layer 51 is typically removed using hot phosphoric acid (H_3PO_4). Silicon nitride layers show relatively low etch rates in phosphoric acid and hence, a poor etch selectivity to polysilicon. Due to the poor etch selectivity of silicon nitride compared to polysilicon, particularly to pre-doped polysilicon, long etch process times are required to reliably remove the buried anti-reflective coating layer. The long process time causes undesired etching of the polysilicon device feature, i.e. the gate electrode 41. Thus, the surface roughness of the gate electrode 41 is increased, possibly to an extent that the shape thereof is altered. Moreover, controlling of the dimensions of the gate electrode 41 may be affected, and consequently, these variations in shape and size may deteriorate the device performance.

Besides the drawback associated with the removal of a buried antireflective coating layer 50 a second drawback in the fabrication of advanced MOS field effect transistor devices is emerging, concerning the removal of disposable sidewall

spacers. Disposable sidewall spacers are required to reduce the Miller (drain/gate) capacitance caused by the LDD/gate-overlap generated in a typical prior art process as described in the following.

The use of sidewall spacers, according to a typical prior art process sequence (without disposable spacers), and the corresponding process flow for forming an MOS-field effect transistor is described with reference to Figs. 2a-2f, wherein features identical to those illustrated in Fig 1a – 1c are denoted by the same reference numerals.

Fig. 2a schematically depicts the semiconductor structure 1 during the lightly doped drain (LDD) implantation process 74. The semiconductor structure 1 comprises the silicon substrate 10, the shallow trench isolation regions 20, the patterned gate insulation layer 31, the gate electrode 41 and a implanted LDD regions 71.

In the fabrication of MOS field effect transistor devices, source and drain regions of the transistor are formed after the formation of the gate electrode 41 in a self-aligning process. The shallow trench isolation regions 20 and the gate electrode 41 define active regions where the LDD implantation is effective. Depending on the type of ions, for example, phosphorus (P) or boron (B), n-type or p-type MOS-field effect transistors, respectively, may be formed. To provide the source and drain regions with the lightly doped drain (LDD) region 71, an according implantation of doping ions is performed.

Fig. 2b depicts the semiconductor structure 1 with a deposited silicon oxide or silicon nitride layer 80. The layer 80 may be blanket-deposited using a well known chemical vapor deposition (CVD) process.

Fig. 2c depicts the semiconductor structure 1 after the formation of sidewall spacers 81.

After the formation of the LDD regions 71, the sidewall spacers 81 are formed to protect the extension regions of the LDD regions 71 and to define a region for the subsequent implantation process carried out to form heavily doped deep

source/drain regions 72 of a source/drain 70 shown in Fig. 2d. The sidewall spacers 81 are formed in an anisotropic etch process, typically in a plasma etch process.

Fig. 2d depicts the semiconductor structure 1 during the deep source/drain implantation process 75. In addition to the semiconductor structure 1 of Fig. 2c, the implanted deep source/drain regions 72 are shown. The sidewall spacers 81 are employed to prevent the implantation of the ions into the extension regions of LDD regions 71 to generate the desired implantation profile.

Fig. 2e depicts the semiconductor structure 1 after performing the subsequent thermal annealing process. Thus, the LDD regions 71 comprise LDD/gate overlap portions 73.

The annealing is required to incorporate the implanted ions into the semiconductor lattice, i. e. to activate the implanted ions, and to repair the damage of the crystal structure caused by the implanted ions. The annealing of the deep source/drain regions 72 and of the LDD regions 71 is typically carried out in a single annealing process. Annealing, however, also causes diffusion of the ions into the surrounding regions having a lower ion density. Due to the high diffusivity required for the deep source/drain annealing, the LDD ions diffuse also laterally under the gate electrode 41 and accordingly extend the LDD regions 71 under the gate electrode 41 and thus form the LDD/gate overlap portions 73. As a consequence, parasitic capacitances (drain/gate capacitance, known as Miller capacitance) are increased and the device performance is further deteriorated.

Fig. 2f depicts the semiconductor structure 1 after the formation of silicide regions 91 in the source/drain regions 70 and on the gate electrode 41.

The silicide regions 91 are formed in a conventional self aligned silicide process. The silicide process may, for example, be performed by blanket-depositing a metal layer and by a subsequent two step thermal annealing process, wherein non reacted excess metal by is removed by an appropriate etch process after the first anneal step.

The undesired diffusion of the dopants of the LDD regions 71 under the gate insulation layer 31 can be prevented or at least reduced by varying the sequence of the process steps. An improved dopant concentration profile of the source/drain regions 70, with a reduced LDD/gate overlap portions 73, may be achieved when the heavily doped deep source/drain regions 72 are implanted and annealed prior to the implantation of the LDD regions 71. Forming the LDD regions 71 after the annealing of the deep source/drain regions 72 permits the optimization of the required second (LDD) annealing process with respect to the LDD activation and lateral dopant diffusion. Varying the sequence of the process as mentioned, however, requires the removal of the sidewall spacers 81 after the formation of the deep source/drain regions 72. Typically silicon nitride (SiN) is employed as a material of the sidewall spacers 81. Due to the poor selectivity of the silicon nitride etch process to the adjacent doped silicon, the removal of the sidewall spacers 81 may lead to a device degradation caused by an incomplete removal of the silicon nitride spacer, thereby affecting subsequent processes, and/or by over-etching, thereby damaging silicon regions of the gate electrode 41 and the source/drain regions 70.

In view of the disadvantages of the conventional removal process of the buried anti-reflective coating layer 50 and/or of the sidewall spacers 81, it is desirable to provide a method allowing the removal of device features without unduly sacrificing adjacent materials and/or negatively affecting subsequent process steps.

SUMMARY OF THE INVENTION

According to the present invention, a method is provided, wherein features of a semiconductor device, which have to be removed, are irradiated by ions to modify the structure of the material of the features in order to enhance the etch rate thereof and to consequently increase the etch selectivity in the corresponding removal process.

According to one illustrative embodiment of the present invention, a method of forming a semiconductor device feature comprises providing a substrate having a first layer formed thereon and covering the substrate with a second layer of

material. Then, ions are implanted into the second layer of material to modify a structure of the material of the second layer and the second layer of material and the first layer by photolithography are patterned to form the semiconductor device feature in the first layer. The patterned second layer of material is then removed, whereby a selectivity in removing the patterned second layer is increased by the implanting of the ions.

According to another illustrative embodiment of the present invention, a method of forming a semiconductor device structure comprises providing a substrate having formed thereon at least one partially completed semiconductor device, wherein the partially completed semiconductor device comprises at least one feature with sidewalls and sidewall spacers formed thereon. The method further comprises implanting ions into the sidedwall spacers, whereby the substrate is tilted with respect to a direction of incidence of the ions. Additionally, the sidewall spacers are removed, whereby a selectivity is increased by the implantation of ions.

BRIEF DESCRIPTION OF THE DRAWINGS

Further advantages, objects and embodiments of the present invention are defined in the appended claims and will become more apparent with the following detailed description when taken with reference to the accompanying drawings, in which:

Figs. 1a – 1d schematically depict a cross sectional view of a semiconductor device structure, illustrating a typical process flow of a gate formation process according to the prior art;

Figs. 2a – 2f schematically depict a cross sectional view of a semiconductor device structure illustrating a typical process flow of the formation of the source/drain regions of a MOS-field effect transistor according to the prior art;

Figs. 3a and 3b schematically depict a cross sectional view of a semiconductor device structure, illustrating the gate formation process in accordance with an illustrative embodiment of the present invention; and

Figs. 4a – 4h schematically depict a cross sectional view of a semiconductor device structure illustrating the formation of the source/drain regions of a MOS-field effect transistor in accordance with one illustrative embodiment of the present invention.

It should be noted that the dimensions shown in the Figures are not true to scale.

DETAILED DESCRIPTION

While the present invention is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present invention to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present invention, the scope of which is defined by the appended claims.

The present invention includes the concept of improving the selectivity of an etch process performed to remove a buried anti-reflective coating layer and sidewall spacers. The selectivity of the etch process is enhanced by increasing the etch rate of the material forming the features to be removed. The etch rate is increased by irradiating ions into the feature. Implanting ions into a solid feature changes the structure of the material of the feature into a more amorphous state, i. e. the short range order in the structure of the material is modified. Particularly heavy ions cause strong damage in the solid structure even at a relatively low dose. In one particular embodiment inert ions are employed so that the electrical characteristics of the implant regions are minimally affected by the implanted ions. Thus, the term "inert ions" is to be understood as referring to ions having only a minimal influence on the electrical behavior of the materials employed to form the device features, and substantially not acting as a dopant in the semiconductor regions. Thus, for example, argon (Ar), xenon (Xe), and the like may be used as inert ions. For silicon-based or germanium-based device features silicon (Si) or germanium (Ge) ions, respectively, may be considered as "inert ions".

With reference to Figs. 3a, 3b and Figs. 4a – 4h, illustrative embodiments according to the present invention will now be described. In Figs. 3a, 3b and 4a – 4h, the same reference signs as in Fig. 1 and 2 are used to denote similar or identical components and parts.

The embodiments illustrated in Figs. 3a, 3b and Figs. 4a – 4h relate to a field effect transistor device formed on a silicon substrate and comprising a polysilicon gate device feature. The substrate employed, however, is not limited to a silicon substrate, and any other substrate, for example, a germanium substrate or a silicon on insulator (SOI) substrate may be used. Moreover, the device feature is not limited to a polysilicon gate, and any other gate or interconnect line feature, for example, a metal gate or a polysilicon interconnect line may be used.

The illustrative embodiments according to the present invention shown in Fig. 3a and 3b employ the same steps as described with respect to Figs. 1a – 1c. The polysilicon gate is formed in the same way except one additional step which is carried out after the deposition of the buried anti-reflective coating layer 50 and prior to the photolithography process. Thus, Figs. 3a and 3b schematically depict only the additional process step and the improved results achieved by the method according to the present invention.

Fig. 3a schematically depicts a semiconductor device structure 1 comprising a silicon substrate 10, shallow trench isolation regions 20 and a gate insulation layer 30. A semiconductor layer 40 and a buried anti-reflective coating layer 50 are formed on the semiconductor device structure 1.

After forming the semiconductor device structure 1 as shown in Fig. 3a by well-known deposition techniques, the semiconductor device structure 1 is, contrary to the conventional process flow, subjected to an ion implantation as indicated by arrows 76. The buried anti-reflective coating layer 50 comprises an inorganic material, for example, silicon nitride (SiN) or silicon reacted nitride (SRN). The entire anti-reflective coating layer 50 is uniformly irradiated by inert ions to modify the structure of the layer 50. That is, the inert ions may destroy or at least significantly change any short-range order of the material in layer 50, thereby

enhancing the diffusivity of particles entering the material. In one embodiment, heavy inert ions, for example, argon and/or xenon, are employed. In another embodiment ions of the same semiconductor type as the material of the semiconductor of layer 40 and/or the substrate 10 are used to substantially avoid altering the electrical characteristic of the semiconductor regions by ions that may penetrate the semiconductor layer 40 and/or the substrate 10 during implantation. In one embodiment, the implant energy is selected such that the structure of the layer 50 is modified substantially throughout the entire thickness of the layer 50. The ion energies are typically in the range from approximately 30 to 200 keV and employed ion doses are typically in the range from approximately $1 \cdot 10^{13}$ to $1 \cdot 10^{15}$ ions/cm².

In other embodiments, only a portion of the thickness of the layer 50 is modified, thereby still enhancing the overall etch rate in a subsequent etch process. In one embodiment the ion energies are selected such that the implanted ions are substantially located in the buried anti-reflective coating layer 50 close to the interface of the buried anti-reflective coating layer 50 and the semiconductor layer 40. The ion energies in these embodiments are typically in the range from approximately 5 to 80 keV.

Fig. 3b schematically depicts the semiconductor device structure 1 after patterning the semiconductor layer 40 and the layer 50, and removing the patterned layer 50. A corresponding process flow may include the steps as described with respect to Fig. 1d. In contrast to the prior art, however, due to the increased etch rate of the layer 50 caused by the irradiation of ions, the etch selectivity of the polysilicon gate electrode 41 relative to the buried anti-reflective coating layer 50 is increased. Thus, the etch process time is reduced and the gate electrode 41 is less affected by the etching process. Thus, the surface roughness and the control of shape and size of the semiconductor device structure 1, particularly of the gate electrode 41, is improved. Advantageously this permits, due to the improved control of shape and size of the device features in the buried ant-reflective coating layer removal process, a second feature removal process may be performed on the same semiconductor structure 1 without an undue degradation of the gate electrode 41. As mentioned in the prior art section of the description, in advanced field effect

transistors it may be necessary to perform a sidewall spacer removal process, to generate source/drain regions with an desired dopant concentration profile.

The selectivity of the etch process to remove the sidewall spacers may also be improved by irradiating ions into the sidewall spacers prior to the etch removal. A corresponding process flow is shown in Figs. 4a – 4h for the semiconductor structure 1 of Fig. 3b.

Fig. 4a schematically depicts the semiconductor device structure 1 comprising the silicon substrate 10, the shallow trench isolation regions 20, the gate insulation layer 31 and the gate electrode 41 as described with respect to Fig. 3b.

Fig. 4b depicts the semiconductor device structure 1 after the deposition of a silicon nitride layer 80. The silicon nitride layer 80 may be deposited in a conventional chemical vapor deposition (CVD) process, for example, in a low pressure chemical vapor deposition (LPCVD) process.

Fig. 4c depicts the semiconductor device structure 1 after formation of sidewall spacers 81 and during an implantation process 77.

The sidewall spacers 81 are formed in a conventional anisotropic plasma etch process. Subsequently, the implantation process 77 for forming the deep source/drain regions 72 is performed. Following the implantation, a deep source/drain rapid thermal annealing (RTA) process is carried out at a high temperature prior to the implantation of the LDD regions. Consequently, the deep source/drain region annealing process may not cause diffusion of the LDD ions and a corresponding undesired LDD/gate overlap may be avoided.

The silicon nitride sidewall spacers 81 may be covered with a thin silicon oxide layer (not shown), particularly when the annealing process takes place in an oxygen containing ambient. The thin silicon oxide layer grows in a slow and self-limiting process by conversion of nitride to oxide.

Fig. 4d depicts the semiconductor device structure 1 after the source/drain implantation. Then a second implantation process 78 is performed wherein the substrate 10 is tilted with respect to the direction of the irradiated ion beam. The tilt angle is chosen to implant a substantial amount of the ions into the sidewall spacers 81. At least a further tilted implantation process 78 is performed to implant ions also into the opposed sidewall spacer 81. The tilt angle is in the range from approximately 10 to 85°. In one embodiment, the employed ions may be heavy inert ions, for example, xenon and/or argon ions. In other embodiments, alternatively or additionally, semiconductor ions, for example silicon or germanium, may be employed. By using germanium ions in a silicon device, it is possible to modify concurrently the band structure of the implant regions on the device, for example, to reduce the substrate floating effect in SOI-MOSFETs. The appropriate ion energy is in the range from approximately 10 to 80 keV and the employed ion doses are typically in the range from approximately $1 \cdot 10^{13}$ to $1 \cdot 10^{15}$ ions/cm². The implanted ions cause damage in the structure of the material of the sidewall spacers 81, thereby increasing the etch rate in the subsequent etch removal process. An increased etch rate of the material of the spacers 81 leads to an improved spacer to semiconductor selectivity in the etch process. Thus the sidewall spacers 81 may be removed without or at least reduced device degradation that would otherwise occur, due to the undesired etching of the gate electrode 41 and of the adjacent deep source/drain regions 72.

In addition, the irradiation of ions also improves the etch rate of the silicon oxide layer (not shown) that may cover the sidewall spacers 81. Thus, the silicon oxide layer may be removed during the silicon nitride etch (spacer removal) process or may be removed in a shorter hydrogen fluoride (HF) dip process compared to the prior art HF dip process.

In another embodiment, the ion implantation 110 into the sidewall spacers 81 may be performed prior to the rapid thermal deep source/drain annealing process, or, in yet another embodiment, prior to the formation of the deep source/drain regions 72. Thus, the crystalline structure of the source/drain regions 72 is more intensively amorphized and allows a more effective curing of lattice damage in the subsequent anneal cycle.

Fig. 4e depicts the semiconductor device structure 1 after annealing and after the removal of the sidewall spacers 81.

Fig. 4f depicts the semiconductor device structure 1 during an implantation process 79 for forming LDD regions 71. The LDD implantation is performed in a conventional implantation process. The subsequent rapid thermal annealing cycle, however, may be advantageously optimized for the required LDD activation whereby concurrently a minimal lateral diffusion is effected. The diffusivity may be reduced compared to an annealing process required when the deep source/drain regions 72 and the LDD regions 71 have to be annealed in a single process. Thus, lateral diffusion of the LDD ions under the gate electrode 41, and hence the formation of LDD/gate overlap portions 73, is avoided or at least reduced as indicated by reference sign 73a. Thereby, the undesired parasitic capacitances are decreased and the device performance is improved.

Fig. 4g depicts the semiconductor device structure 1 after sidewall spacers 82 are formed. The newly formed sidewall spacers 82 allow a self-aligned silicide formation.

Fig. 4h depicts the semiconductor device structure 1 after the formation of silicide regions 91 on the source/drain regions 70 and on the gate electrode 41. The silicide process may be performed as described with reference to Fig. 2f. The semiconductor device structure 1 shows an improved source/drain dopant concentration profile and thus, an improved device performance.

The method of improving the etch behavior of the material of sidewall spacers 81 by implantation of ions may also be employed for field effect transistors comprising a thin liner oxide (not shown) on the gate- and on the source/drain electrodes. In such a device, the sidewall spacers 81 are consequently formed on the liner oxide. Although, the etch selectivity of silicon nitride to silicon oxide is better than the selectivity of silicon nitride to silicon or polysilicon, controlling of critical dimensions may also be improved in devices comprising a liner oxide.

Further modifications and variations of the present invention will be apparent to those skilled in the art in view of this description. Accordingly, the description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the present invention. It is to be understood that the forms of the invention shown and described herein are to be taken as the presently preferred embodiments. It should be further noted that the embodiments described above may be combined with each other in any appropriate manner.

CLAIMS

1. A method of forming a semiconductor device feature, the method comprising:

providing a substrate having a first layer formed thereon;

covering the substrate with a second layer of material;

implanting ions into the second layer of material to modify a structure of the material of the second layer;

patterning the second layer of material and the first layer by photolithography to form the semiconductor device feature in the first layer; and


removing the patterned second layer of material, whereby a selectivity in removing the patterned second layer is increased by the implanting of said ions.

2. The method of claim 1, wherein the ions are substantially inert ions.
3. The method of claim 1, wherein the ions are at least one of argon ions, xenon ions, germanium ions and silicon ions.
4. The method of claim 1, wherein the ion dose is in the range from approximately $1 \cdot 10^{13}$ to $5 \cdot 10^{15}$ ions/cm²
5. The method of claim 1, wherein the ion energy is in the range from approximately 5 to 80 keV.
6. The method of claim 1, wherein the layer of material is an antireflective coating layer.
7. The method of claim 1, wherein the layer of material is comprised of an inorganic material.

8. The method of claim 1, wherein the material of the layer of material is one of silicon nitride and silicon reacted nitride.

9. The method of claim 1, wherein a dimension of the device feature in one direction is 100 nm or less.

10. A method of forming a semiconductor device structure, the method comprising:




providing a substrate having formed thereon at least one partially completed semiconductor device, wherein the partially completed semiconductor device comprises at least one feature with side walls and side wall spacers formed thereon;

implanting ions into the side wall spacers by performing an angled ion implantation process;

removing the patterned layer of material, whereby a selectivity in removing the patterned layer is increased by the implanting said of ions.

11. The method of claim 10, wherein providing a substrate further comprises:



forming the sidewall spacers at the sidewalls of the at least one feature of the partially formed semiconductor device by covering the substrate with a layer of material and by patterning the layer of material in an anisotropic etch process.

12. The method of claim 11,

wherein providing a substrate further comprises forming the sidewall spacers at the sidewalls of the at least one feature of the partially formed semiconductor device; and

wherein the method further comprises implanting dopants into the substrate to form a region of enhanced conductivity in the semiconductor device after the

formation of side wall spacers.

13. The method of claim 12, wherein the region of enhanced conductivity comprises at least source/drain regions.

14. The method of claim 10, wherein a tilt angle between a surface of the substrate and the direction of incidence of the ions is in the range from approximately 10 to 85°.

15. The method of claim 10, wherein the ions are substantially inert ions.

16. The method of claim 10, wherein the ions are at least one of argon ions, xenon ions, germanium ions and silicon ions.

17. The method of claim 10, wherein the ions dose is in the range from approximately $1 \cdot 10^{13}$ to $5 \cdot 10^{15}$ ions/cm²

18. The method of claim 10, wherein the ions energy is in the range from approximately 10 to 80 keV.

19. The method of claim 10, wherein the material of the side wall spacers comprises an inorganic material.

20. The method of claim 10, wherein the material of the side wall spacers comprises silicon nitride.

21. The method of claim 10, wherein a dimension of the at least one feature in one direction is 100 nm or less.

ABSTRACT

A method for improving the etch behavior of disposable features in the fabrication of a semiconductor device is disclosed. The semiconductor device comprises a buried anti-reflective coating layer and/or a disposable sidewall spacer, which are to be removed in a subsequent etch removal process. The buried anti-reflective coating layer and/or the disposable sidewall spacer are irradiated by heavy inert ions to alter the structure of the irradiated features and to increase concurrently the etch rate of the employed materials, for example, silicon nitride (SiN) or silicon reacted nitride (SRN).

FIG.1a
(prior art)

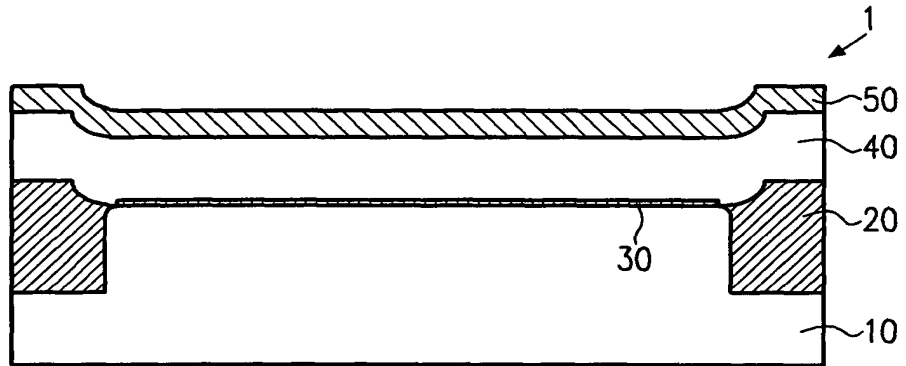


FIG.1b
(prior art)

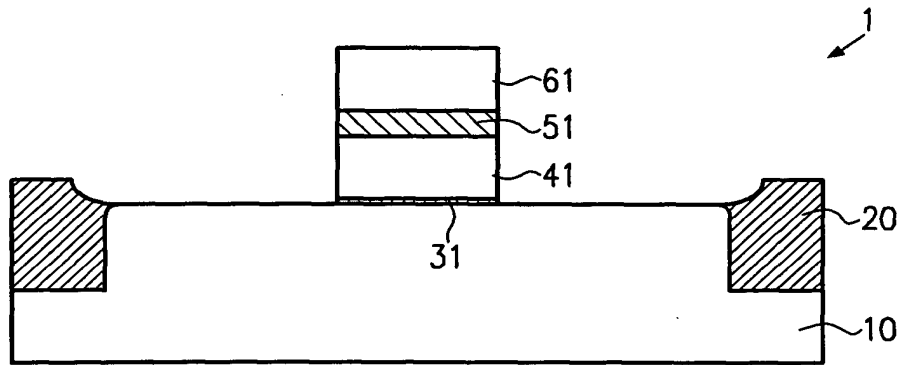


FIG.1c
(prior art)

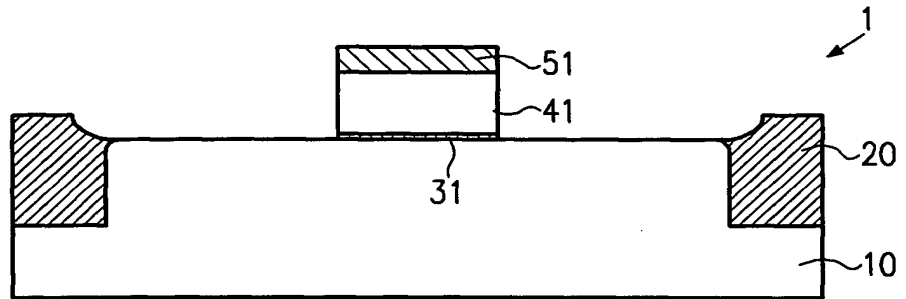
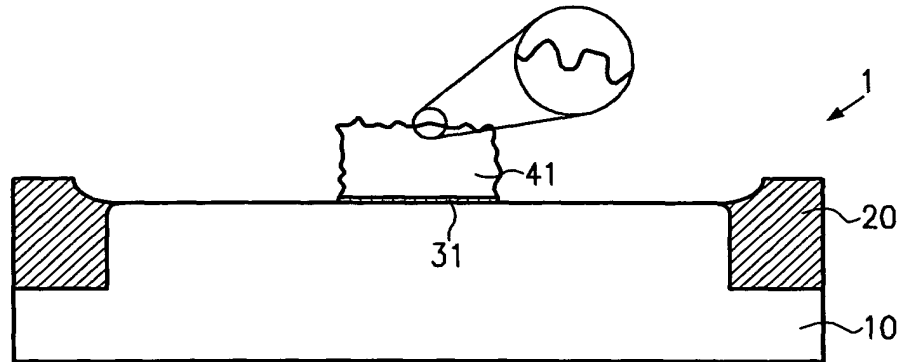


FIG.1d
(prior art)



2/5

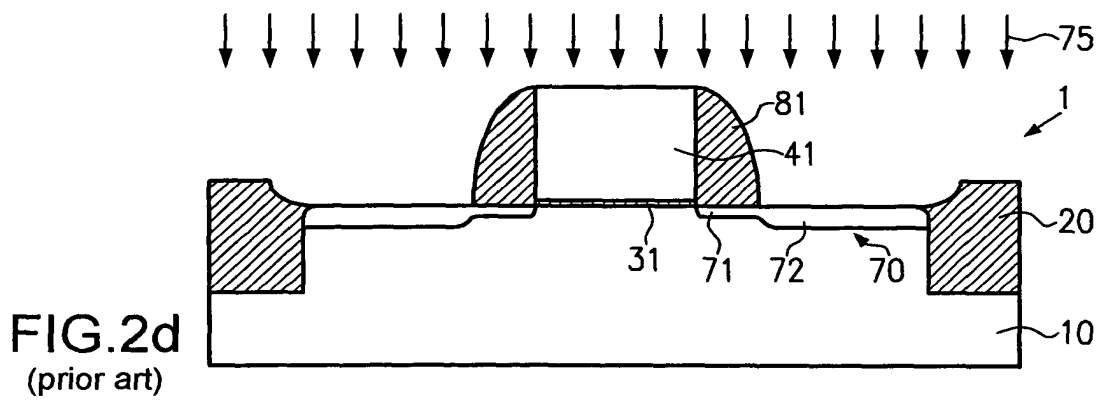
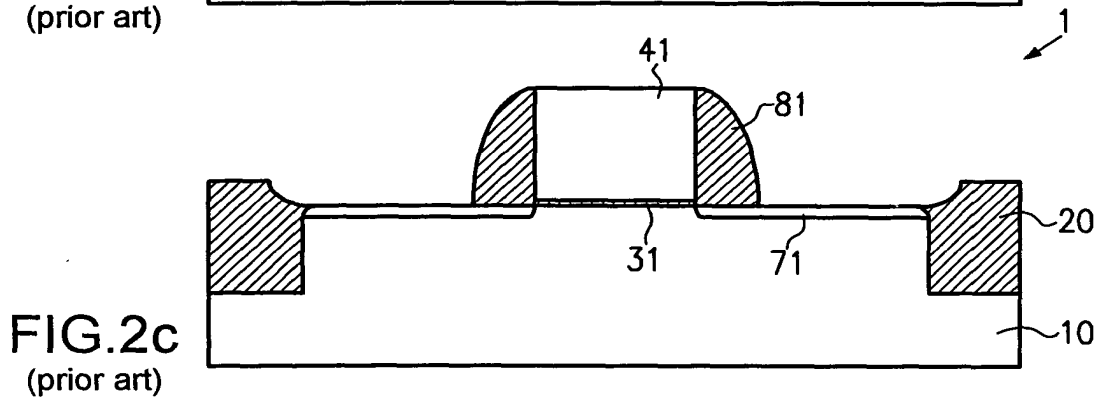
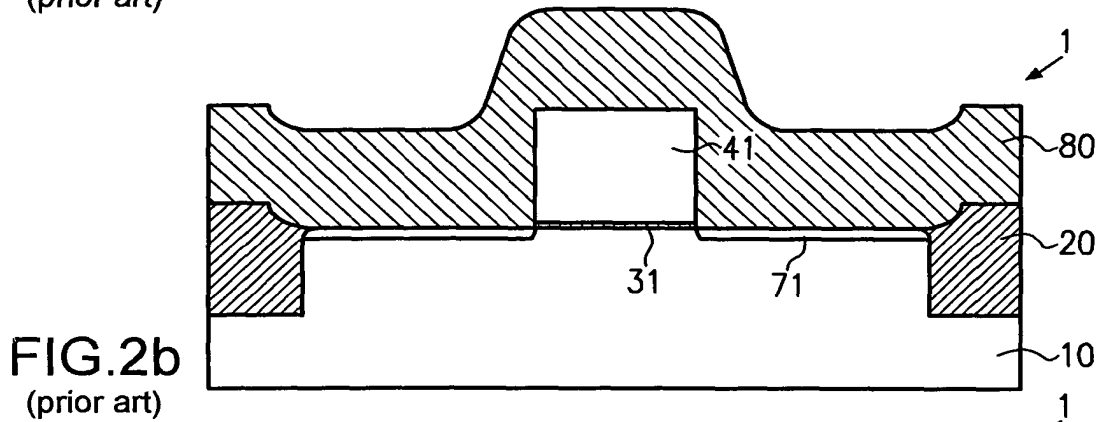
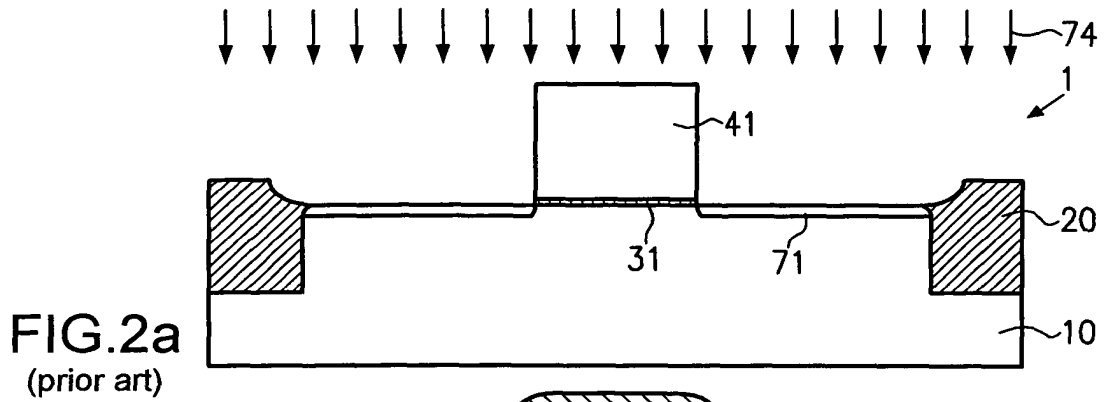


FIG.2e
(prior art)

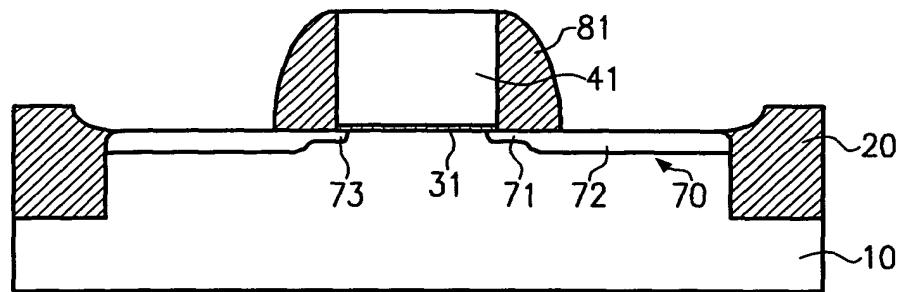


FIG.2f
(prior art)

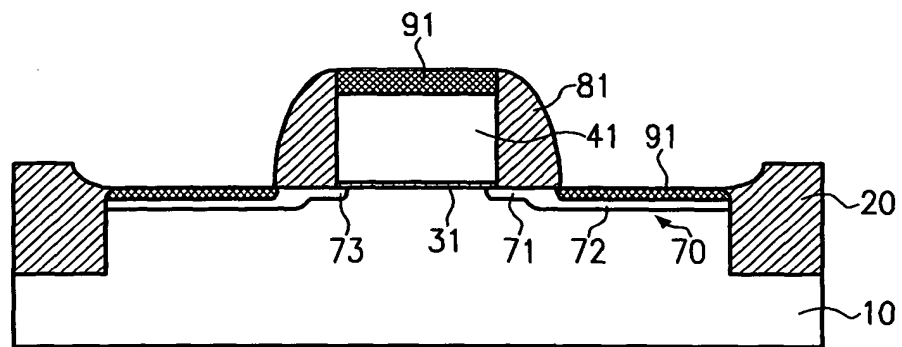


FIG.3a

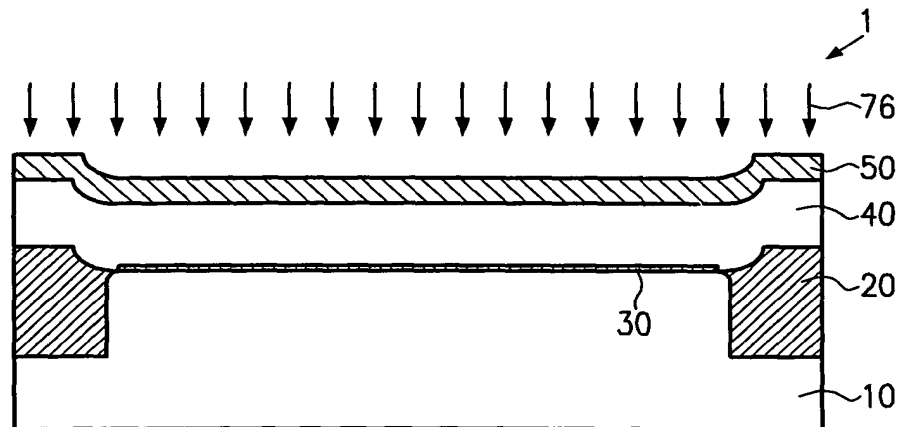


FIG.3b

